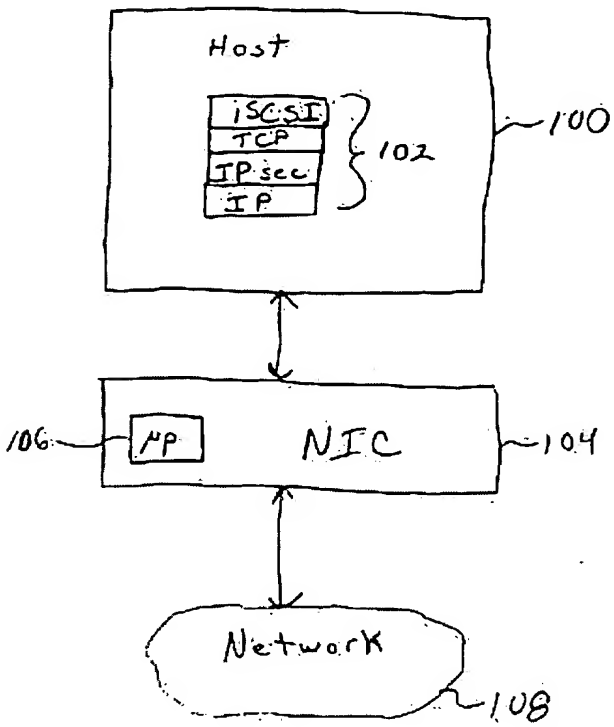


Fig. 1 (prior art)

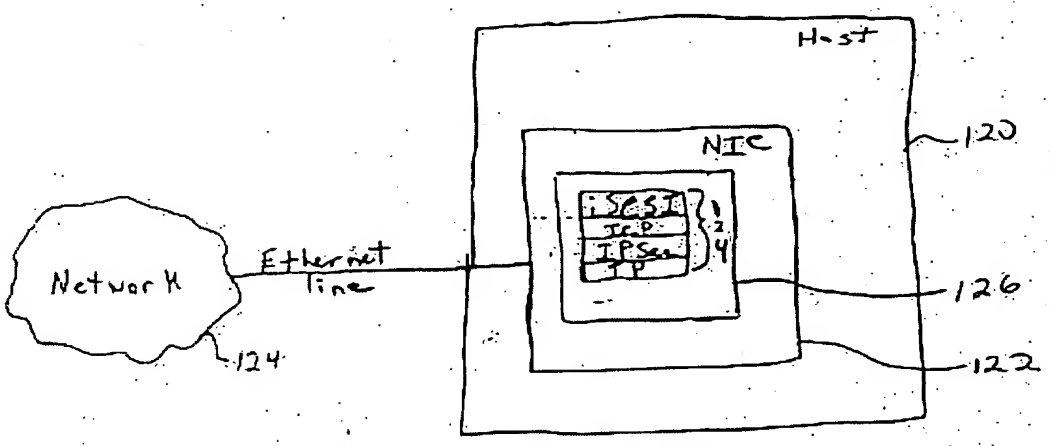

Host
NIC
iSCSI
TCP
IPSec
IP
1
2
4
120
126
122
Network
Ethernet Line
124

Fig. 2

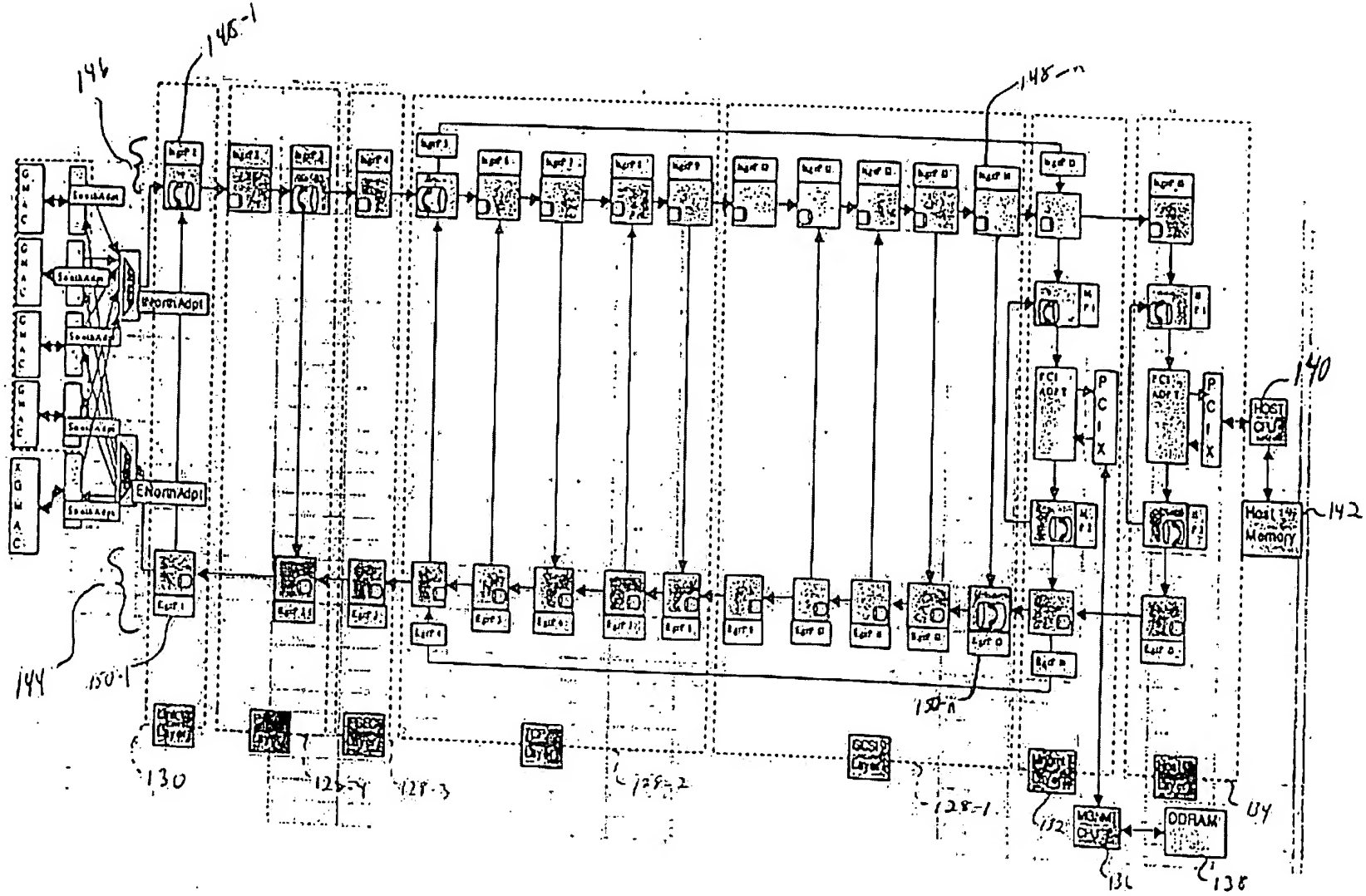
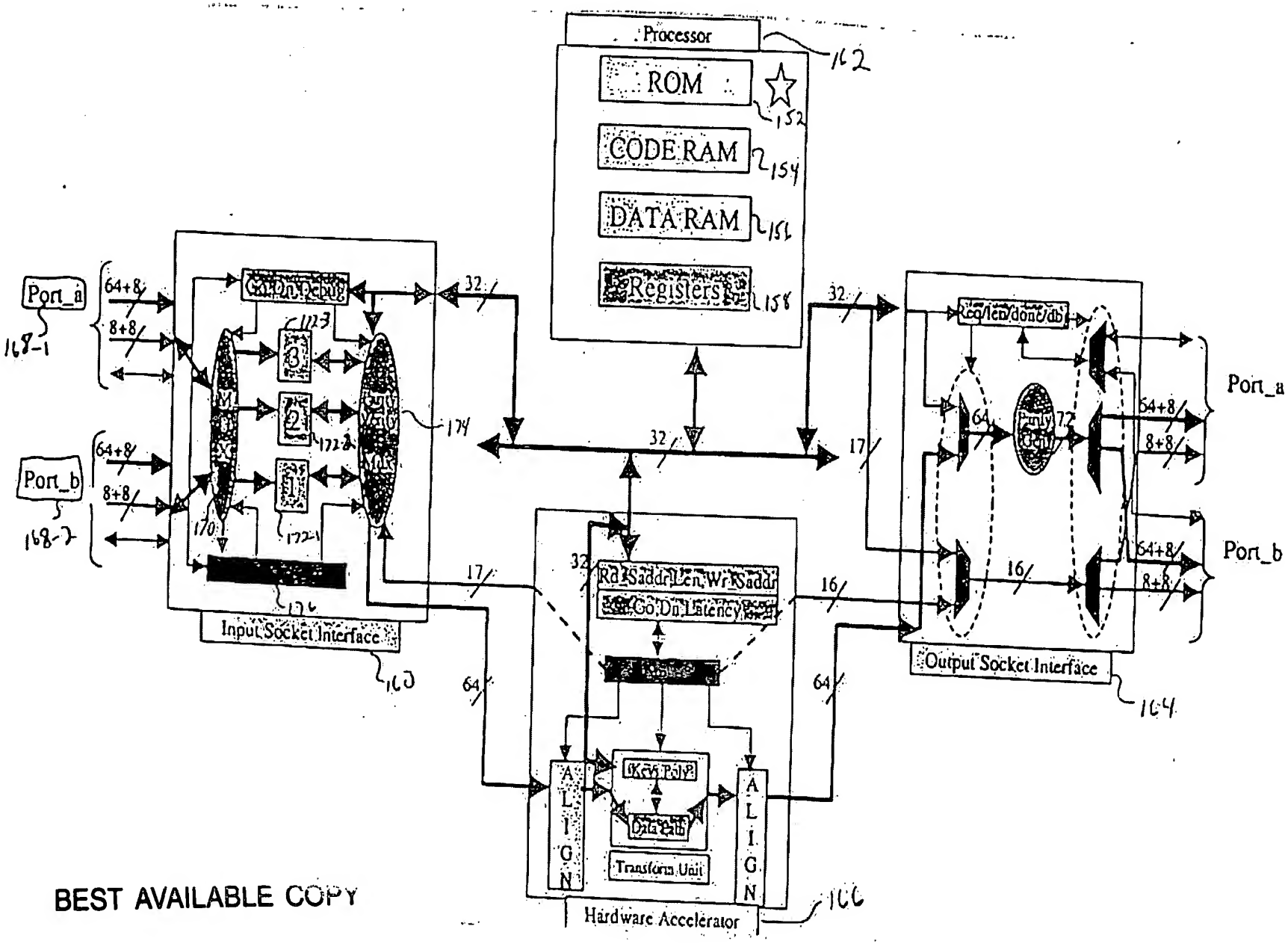


Fig. 3

BEST AVAILABLE COPY



BEST AVAILABLE COPY

Fig 4

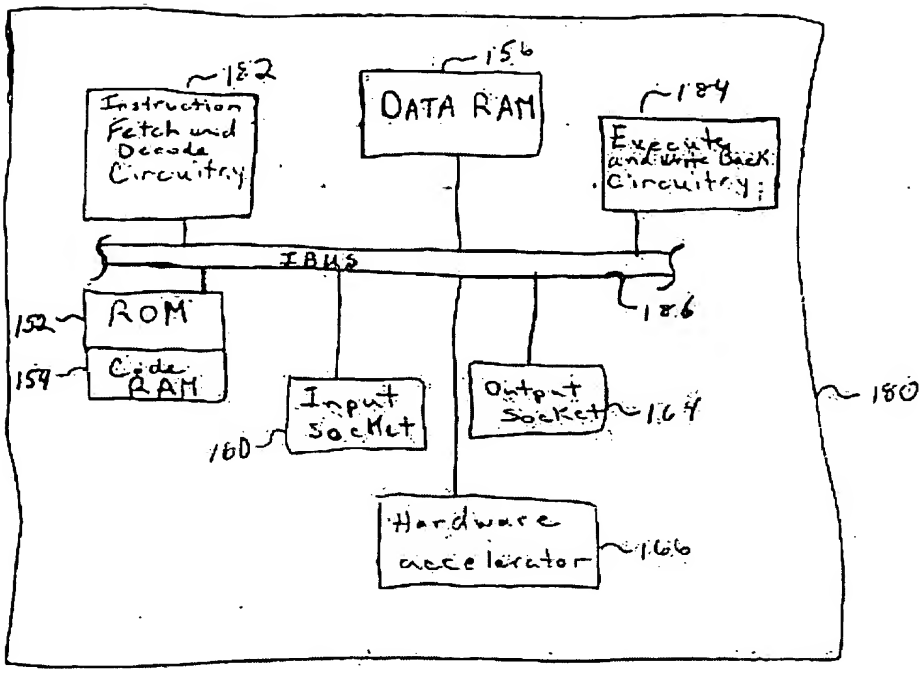
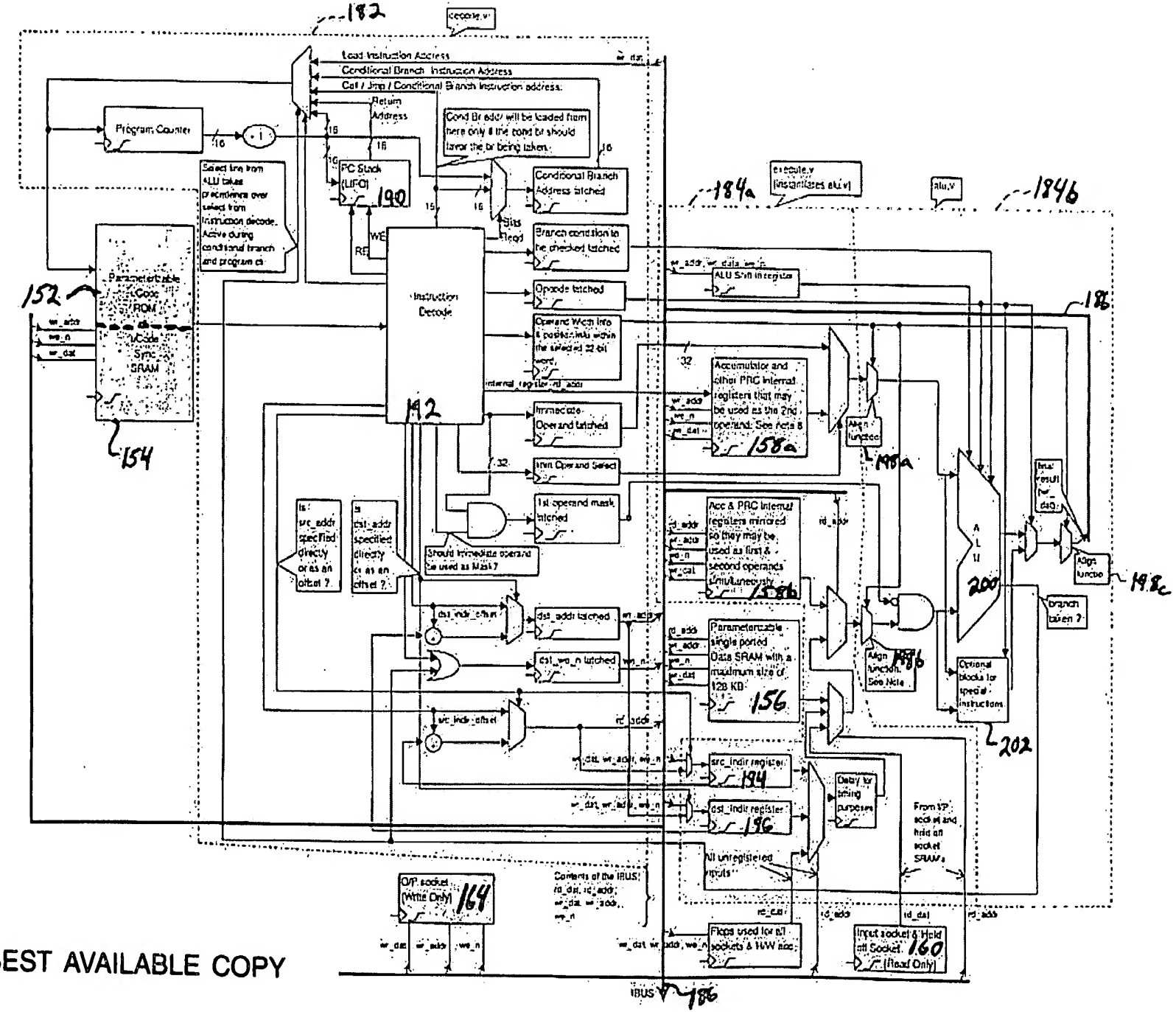

182
Instruction Fetch and Decode Circuitry
156
DATA RAM
184
Execute and write Back Circuitry
IBUS
186
ROM
152
Code RAM
154
Input Socket
160
Output Socket
164
180
Hardware accelerator
166

Fig 5



BEST AVAILABLE COPY

Fig. 6

I - instruction fetch and decode
II - execute and write back.

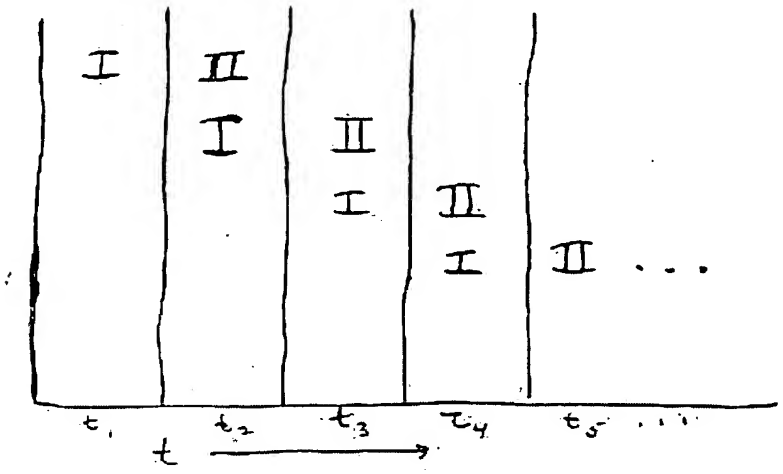


Fig. 7

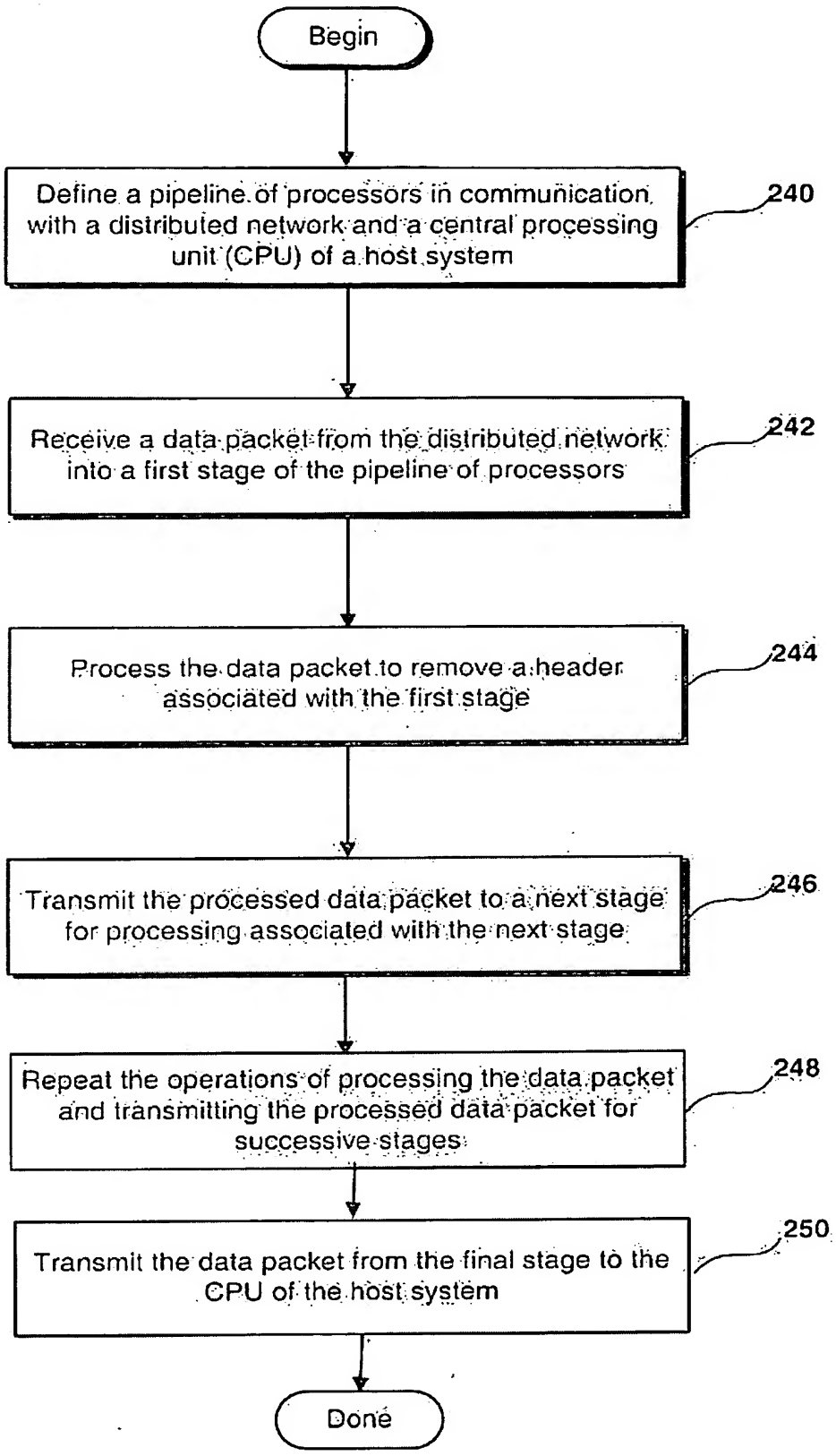

Begin
Define a pipeline of processors in communication with a distributed network and a central processing unit (CPU) of a host system
240
Receive a data packet from the distributed network into a first stage of the pipeline of processors
242
Process the data packet to remove a header associated with the first stage
244
Transmit the processed data packet to a next stage for processing associated with the next stage
246
Repeat the operations of processing the data packet and transmitting the processed data packet for successive stages
248
Transmit the data packet from the final stage to the CPU of the host system
250
Done

Fig. 8